



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,104	12/23/2003	Mitsuhiko Ogihara	MAE 305	8001
23995	7590	06/15/2005	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			MONDT, JOHANNES P	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/743,104

Applicant(s)

OGIHARA ET AL.

Examiner

Johannes P. Mondt

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6,9,10,16-20 and 26-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,9,10,16-20 and 29-34 is/are rejected.
- 7) ☒ Claim(s) 5,6 and 26-28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12/23/03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species 1 in the reply filed on 4/14/05 is acknowledged.

Response to Amendment

Preliminary Amendment filed 4/14/05 together with aforementioned election forms the basis for this office action. In said Preliminary Amendment Applicant cancelled claims 7, 8, 11-15 and 21-25 and added new claims 26-34.

Claim Objections

2. **Claim 31** is objected to because of the following informalities: the wording "said electrically conductive layer" should be replaced by "an electrically conductive layer" (line 4).. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-4 and 19** are rejected under 35 U.S.C. 102(b) as being anticipated by Ryou (5,492,851). Ryou teaches (Figure 2E, title, abstract, and cols. 2-4) a combined semiconductor apparatus (diverse device components including field effect transistors and capacitors are discussed in the abstract) comprising: a semiconductor substrate 1

Art Unit: 2826

(col. 2, l. 62) having an integrated circuit (field effect transistor has gate 4 and hence has integrated circuit)(col. 3, l. 1-10) most adjacent said bit line electrode 13 (col. 3, l. 39); a planarized region 7/12/14 (col. 3, l. 40-43 and col. 3, l. 13-32) formed in a surface of said semiconductor substrate; and a semiconductor thin film 15 (col. 3, l. 47 – col. 4, l. 4) including at least one semiconductor device (thin film MOSFET with gate 17 (col. 3, l. 65) (cf. col. 4, l. 1) and bonded on said planarized region by virtue of being deposited onto it, inherently so because of the adhesive chemical bonding between deposited (15) and underlying (14) material. In conclusion, Ryou anticipates claim 1.

On claim 2: said planarized region is a part of said surface of said semiconductor substrate (when taken as a two-dimensional region: this is necessary as otherwise the limitation would not make any sense: a three-dimensional region can never be part of a surface, as any surface has dimension less than three) that has been subjected to a planarizing process (col. 3, l. 40-43). The examiner also herewith makes of record that whether or not a certain process has taken place by itself, - as opposed to the structural consequences of said process, is of no patentable weight in the present device invention.

On claim 3: said planarized region is disposed above said integrated circuit of said semiconductor substrate, because region 7/12/14 is above said transistors with gates 4 adjacent first bit line electrode 13 (cf. Figure 2E).

On claim 4: said planarized region is also disposed in a region of said semiconductor substrate that is adjacent to said integrated circuit of said semiconductor

substrate (adjacent = "near"; with reference to Merriam-Webster's Collegiate Dictionary, 10th Ed., page 14).

On claim 19: said at least one semiconductor device is a single semiconductor device disposed in said semiconductor thin film, namely: a thin film MOSFET transistor with gate 17.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. ***Claims 1, 9, 10, 16-18, 20, 29-31 and 33-34*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2003/0067043 A1) in view of Muto et al (JP 61102767 A). Zhang teaches a combined semiconductor apparatus (three-dimensional IC memory integrated with an embedded read-write memory (eRWM): title, abstract and [0023]-[0024]) comprising: a substrate having an integrated circuit (0s) ([0074]); a planarized region (all regions below 23: in view of the stated planarization step after filling with dielectric 26 as discussed in [0102] the region below 23 is planarized) ([0102]-[0103]) formed in a surface of said substrate (Figures 9 and 10BA); and a semiconductor thin film (either 20a or 30a2: ([0109]) including at least one semiconductor device (P+/N-/N+ diode) and bonded on said planarized region (Figure 10BA; in the case of 30a2 this bonding is indirect but present through 20a). Zhang does not necessarily teach said substrate to be a semiconductor substrate. However, as

witnessed by Muto et al, a compound semiconductor substrate of semi-insulating GaAs is advantageous because it allows read and write operations to be conducted at high speed (see English abstract). *Motivation* to include the teaching by Muto et al stems directly from the high read/write speed considering the eRWM component in the device by Zhang.

On claim 9: said semiconductor thin film as selected to be 30a2 has a common electrode layer 20a on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor film, in which said semiconductor device is formed (first surface is upper main surface, second surface is lower main surface, of 30a2) (cf. Figure 10BA), and said second surface of said semiconductor thin film is disposed on a side of said planarized region of said semiconductor substrate (because said semiconductor substrate with planarized region is below said semiconductor thin film (cf. Figure 10BA).

On claim 10: said integrated circuit includes individual electrode terminals (source/drain terminal are inherent to the transistors 0T,...,(Figure 2A); said apparatus further comprising individual interconnecting lines 20av, 30av,..., formed on a region extending from an upper surface of said semiconductor device to said individual electrode terminals (cf. Figure 2A and [0074]).

On claim 16: Zhang does not necessarily teach said semiconductor film to be made of a compound semiconductor as main material. However, it would have been obvious to do so in view of Muto et al, who teach to use a wide band gap semiconductor for high read/write operation speed. Said high speed is due to the higher electron

mobility in GaAs in comparison with silicon. Motivation, to include the teaching by Muto et al, stems directly from the high read/write speed, considering the eRWM component in the device by Zhang.

On claim 17: said at least one semiconductor device, being part of the eRWM, inherently is a light-emitting element (laser diode) for read/write operations and said integrated circuit includes a driving-IC for driving said at least one semiconductor device (namely: the driver circuitry inherently present within the logic block present at each level: see [0012]).

On claim 18: said at least one semiconductor device is a plurality of semiconductor devices arranged in said semiconductor thin film, the memory cell 110 being merely a member of a memory array with the semiconductor thin film 20a connecting members on the same row ([0074] and [0109]).

On claim 20: as discussed above, the diode discussed above is a laser diode for read and write functions, the write function implying it to be an optical print head.

On claim 29: a first surface of said semiconductor thin film taken as 30a, in which said semiconductor device is formed, is disposed on a side of said semiconductor substrate (cf. Figure 2A), namely on the upper main side of said semiconductor substrate (Figure 2A).

On claim 30: restricting to the alternative discussed above of 30a2 as the semiconductor thin film the combined semiconductor apparatus by Zhang further comprises an electrically conductive layer disposed between said semiconductor substrate and said semiconductor thin film, namely 20a ([0101] and [0109]-[0110]).

On claim 31: subject to the objection to this claim formulated above under Claim Objections: the apparatus by Zhang et al further comprises an inter-dielectric layer 23 disposed between said semiconductor substrate and said semiconductor thin film (see [0109]) and in a region peripheral to an electrically conductive layer 20a (see [0109] and Figure 10BA) ("said electrically conductive" misunderstands there to be such a layer within the context of claim 31 including 29 (as opposed to claim 30)).

On claim 33: as discussed above, the diode discussed above is a laser diode for read and write functions, the write function implying it to be an optical print head.

On claim 34: Zhang teaches an image-forming apparatus comprising at least one optical print head including the combined semiconductor apparatus of claim 29, because said apparatus is a computer-on-chip integrating a 3D-M (memory device) with embedded processor and embedded read-write memory in the form of PonC, which is capable of playing contents including audio/video materials (see [0026]).

7. **Claim 32** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang and Muto et al as applied to claim 29 above, and further in view of Puar (4,342,102).

As detailed above, claim 29 is unpatentable over Zhang in view of Muto et al. Furthermore, said semiconductor thin film in Zhang includes a common electrode layer 20a ([0109]) on a second surface of said semiconductor thin film opposed to said first surface (namely on the other side than the one at which the semiconductor device is formed), and said integrated circuit has at least several source electrode terminals. Zhang does not necessarily teach said source electrode terminals to have a common voltage thus teaching the integrated circuit to have a common terminal. However, as

evidenced by Puar in the art of memory arrays one common ground potential suffices for all source terminals (col. 2, l. 30-35). Motivation to include said teaching at least derives from the circumstance that voltages only have physical significance as differences and furthermore because the common ground potential saves additional cost otherwise needed to provide each source with a different voltage.

Allowable Subject Matter

8. ***Claims 5, 6 and 26-28*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

(a) with regard to claims 5 and 6: within the context of independent claim 1 the additional film 23 in Zhang et al disposed between the planarized region and the semiconductor film but no mention is made of how *planar* said layer 23 is.

(b) with regard to claims 26-28: within the context of independent claim 1 said raised layer with another semiconductor thin film bonded to its upper surface has not been found.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

Art Unit: 2826

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM

June 12, 2005

Patent Examiner:

A handwritten signature in black ink, appearing to read 'J. Mondt', with a stylized flourish at the end.

Johannes Mondt (Art Unit: 2826)